AMENDMENTS TO THE SPECIFICATION

Please amend the paragraph at page 9, lines 13-21 as follows:

FIG. 2a is a block diagram of an embodiment of a driver circuit **100**, i.e., an[[d]] addressing structure. The driver circuit **100** illustrates a particular detailed implementation of the addressing structure **10** of **Fig 1a**. The circuit **100** is configured to connect voltages to [[323]]324 column electrodes. each electrode connected to a column of switch circuits, such as pixel transistors. The driver circuit **100** includes a voltage rail switch unit **110** (related to the switch unit **12** shown in **FIG. 1a**), voltage rail sources **150** in communication with the voltage rail switch unit **110**, and a data latch **120**, a data register **130** and a 162-bit shift register **140** (the last three being related to the voltage selector **12** shown in **FIG. 1a**[[.]]).

Please amend the paragraph at page 9, line 28 to page 10, line 9 as follows:

The driver circuit **100** provides 324 pixel addressing voltage outputs, one for each of the 324 column electrodes. Each column electrode permits addressing of pixel electrodes attached to the column. The voltage rail sources **150** include 31 rails each providing different voltage levels. The driver circuit **100** is thus capable of applying 31 different output voltage levels ~~(plus a 32nd level of zero volts)~~ to each of the 324 outputs, by selecting a voltage rail **150** having a desired voltage. The voltage levels are a reference voltage Vcom, 15 voltages greater than Vcom (positive voltages), and 15 voltages less than Vcom (negative voltages.) Each voltage level is provided by a corresponding power rail **150** that is in communication with the voltage rail switch unit **110**.

Please amend the two paragraphs at page 13, lines 7-17 as follows:

When the data latches **121** receive the rising edge of a slow clock pulse, Clock 2, the latches **121** write the latched values into the multiplexing units **111**. Each of the multiplexing units **111** has a single output (designated "1," in **FIG. [[1B]]2B**, and held permanently high during typical operation of the circuit **100**) and 32 outputs, one of

which is held high and all the others low. The selected high output depends on the value written into the multiplexing unit **111** by the data latch **121.**

Each multiplexing unit **111** controls to which of the 31 possible input voltages sources **150**, V+(1-15), Vcom and V-(1-15), its associated output line, i.e., **Y001-Y324**, is connected. The different between the 32 possible outputs of each multiplexing unit **111** and the 31 possible input voltages is accommodated by permitting two different outputs of a multiplexing unit to both select [[a]] the Vcom voltage rail **150**.

Please amend the paragraph at page 15, lines 10-18 as follows:

The addressing structure **200** utilizes an address cycle (one frame) of 160 ms, which is divided into 4 sub-frames of 40 ms each. The source drivers **210** select one of the three voltage rails **215a, 215b, 215c** in response to a magnitude bit and a sign bit loaded from the sequencer **220** for each output line. The addressing structure **200** sequences the voltage supplied to the voltage rails **215a, 215b, 215c**, via switching instructions from the sequencer **220**, as each sub-frame of addressing occurs. One power rail ~~215a~~**215b** provides a voltage of Vcom, and the positive rail **215a** and the negative rail **215c** are switched from sub-frame to sub-frame, e.g., switched from V to V/2 to V/4 to V/8.

Please amend the paragraph at page 19, lines 8-15 as follows:

FIG. 4a is a schematic diagram of an embodiment of an addressing structure **300** for a display that includes one or more pixels. The structure **300** includes a resistive switch **320** and a capacitive element **335** associated with each pixel. The capacitive element **335** may be, for example, a capacitor formed in part from a pixel electrode. The resistive switch **320** may be, for example, a transistor. The addressing structure **300** also includes a voltage source **314**, an addressing voltage controller **330** in communication with the voltage source **314**, and the resistive switch **320**.

Please amend the paragraph at page 19, lines 19-24 as follows:

The addressing voltage controller **330** provides a voltage Vd(t) to the resistive circuit **320** in response to an addressing impulse identified by a display signal.

The voltage Vd(t) may be a column drive voltage directed to a column of pixels. A selection voltage Vg(t) may be applied to the resistive circuit **320** if it is, for example, a FET, to switch the resistive circuit **320** to an active, i.e., on, state; the voltage Vd(t) is then applied to the capacitive element **335** to cause it to gradually charge.

Pleases amend the two paragraphs at page 20, lines 14-28 as follows:

FIG. 4b is a flowchart of an embodiment of a method **400** for addressing a display, as can be implemented, for example, by the addressing structure [[**200**]]**300** described above with reference to **FIG. 4a**. The method **400** includes providing a capacitive element, e.g., element **335**, to apply an addressing voltage to a portion of a display medium (**Step 410**), providing a voltage source having a voltage greater than the addressing voltage (**Step 420**), and charging the capacitive element with the voltage source until the capacitive element applies the addressing voltage (**Step 430**).

Each row of capacitive elements of a display may be addressed once per scan of the entire display. For example, a gate driver for each row of pixel FETs activates the TFTs in that [[rwo]]row once per scan. The addressing structure may be configured so that one line time, e.g., the amount of time a gate driver activates a single gate row, is enough to charge the capacitive element to a high percentage of its final value, e.g., 5RC. Thus, the final value effectively is a fully charged pixel capacitive element, i.e., the voltage of the capacitive element is effectively equal to the addressing voltage.